metal layers.

C1 amd.

2. (Twice Amended) The semiconductor device according to claim 1, wherein the connection metal layer and the layer to be connected intersect in the connection area.

6. (Amended) The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the partitioned intermediate metal layers are formed in accordance with minimum design rules in a direction that is orthogonal to the priority wiring direction of the intermediate metal layer.

C2

Add the following new claims 22-30:

22. (Added) The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the intermediate metal layer wiring area is formed in a priority wiring direction in the intermediate metal layer.

C3

23. (Added) The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein appropriate partitioned areas of the intermediate metal layers are secured and the intermediate metal layer wiring areas are formed by deleting appropriate interlayer connection portions that connect the metal layers forming the stack VIA portion.

24. (Added) The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the interlayer connection portions are arranged in an array configuration that matches wiring tracks running in the priority wiring direction in the intermediate metal layers connected to the interlayer connection portions, and are detected where appropriate in row units running in the priority wiring direction.

25. (Added) The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the portioned intermediated metal layers are formed in accordance with minimum design rules in a direction that is orthogonal to the priority wiring direction of the intermediate metal layer.

26. (Added) The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the layer to be connected is a metal layer.

27. (Added) The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the layer to be connected is a non-metal layer.

28. (Added) The semiconductor device having a multiple layer wiring and a stack VIA according to claim 19, wherein the non-metal layer is polycrystalline silicon layer.

29. (Added) The semiconductor device having a multiple layer wiring and a stack VIA

according to claim 19, wherein the non-metal layer is a diffusion layer.

30. (Added) A semiconductor device having a multiple layer wiring and a stack VIA comprising:

a connection metal layer;

a layer to be connected with the connection metal layer;

one or more intermediate metal layers to be provided between the connection metal layer and the layer to be connected; and

a connection area for connecting the connection metal layer and the layer to be connected,

wherein the intermediate metal layer in the connection area is partitioned into two or more partitioned intermediate metal layers, at least one partitioned intermediate metal layer for wiring.